Amendments to the Claims:

Please add new claims 28-30.

Please amend the claims according to the following listing of claims.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A level shifting device, comprising:

a first transistor having its gate connected to an input signal, its source connected to a voltage node at a lower voltage value, and its drain connected to an output signal;

a second transistor having its gate connected to an inverted version of the input signal, its source connected to the voltage node at the lower voltage value, and its drain connected to an inverted version of the output signal;

a third transistor having its gate connected to the drain of the second transistor, and its drain connected to the drain of the first transistor;

a fourth transistor having its gate connected to the drain of the first transistor, its drain connected to the drain of the second transistor, and its source connected to a voltage supply at a first upper voltage value; [[and]]

a fifth transistor having its gate connected to the input signal, its source connected to the voltage supply at the first upper voltage value, and its drain connected to the source of the third transistor;

a sixth transistor connected between the fourth transistor and the voltage supply at the first upper voltage value, the inverted version of the input signal being applied to the gate of the sixth transistor; and

a seventh transistor connected in parallel with the third transistor between the fifth transistor and the first transistor, the inverted version of the input signal being applied to the gate of the seventh transistor;

wherein the input signal swings between a second upper voltage value and the lower

voltage value and the output signal swings between the first upper voltage value and the lower voltage value.

2. (Original) The level shifting device of claim 1, wherein the first transistor is a NMOS transistor, the second transistor is a NMOS transistor, the third transistor is a PMOS transistor, the fourth transistor is a PMOS transistor, and the fifth transistor is a PMOS transistor.

3. (Canceled)

4. (Currently Amended) The level shifting device of claim [[3]] 1, wherein the sixth transistor is a PMOS transistor, the first transistor is a NMOS transistor, the second transistor is a NMOS transistor, the third transistor is a PMOS transistor, the fourth transistor is a PMOS transistor, and the fifth transistor is a PMOS transistor.

5. (Currently Amended) The level shifting device of claim [[3]] 1, wherein the lower voltage value is ground level.

6. (Canceled)

7. (Currently Amended) The level shifting device of claim [[6]] 1, wherein the seventh transistor is a NMOS transistor, the first transistor is a NMOS transistor, the second transistor is a NMOS transistor, the third transistor is a PMOS transistor, the fourth transistor is a PMOS transistor, the fifth transistor is a PMOS transistor, and the sixth transistor is a PMOS transistor.

8. (Currently Amended) The level shifting device of claim [[6]] 1, further comprising an eighth transistor connected in parallel with the fourth transistor between the sixth transistor and the second transistor, the input signal being applied to the gate of the eighth

transistor.

9. (Original) The level shifting device of claim 8, wherein the eighth transistor is a NMOS transistor, the first transistor is a NMOS transistor, the second transistor is a NMOS transistor, the third transistor is a PMOS transistor, the fourth transistor is a PMOS transistor, the fifth transistor is a PMOS transistor, the sixth transistor is a PMOS transistor, and the seventh transistor is a NMOS transistor.

10. (Canceled)

11. (Currently Amended) The level shifting device of claim [[10]] 28, wherein the sixth transistor is a NMOS transistor, the first transistor is a NMOS transistor, the second transistor is a NMOS transistor, the third transistor is a PMOS transistor, the fourth transistor is a PMOS transistor, and the fifth transistor is a PMOS transistor.

12. (Currently Amended) The level shifting device of claim [[10]] 28, further comprising a seventh transistor connected in parallel with the fourth transistor between the second transistor and the voltage supply at the first upper voltage value, the input signal being applied to the gate of the seventh transistor.

13. (Original) The level shifting device of claim 12, wherein the seventh transistor is a NMOS transistor, the first transistor is a NMOS transistor, the second transistor is a NMOS transistor, the third transistor is a PMOS transistor, the fourth transistor is a PMOS transistor, the fifth transistor is a PMOS, and the sixth transistor is a NMOS transistor.

14. (Currently Amended) A level shifting device, comprising:

a first transistor having its gate connected to an input signal, its source connected to a voltage node at a lower voltage value, and its drain connected to an output signal;

a second transistor having its gate connected to an inverted version of the input signal, its source connected to the voltage node at the lower voltage value, and its drain connected to an inverted version of the output signal;

a third transistor having its gate connected to the drain of the second transistor, and its drain connected to the drain of the first transistor;

a fourth transistor having its gate connected to the drain of the first transistor, its drain connected to the drain of the second transistor, and its source connected to a voltage supply at a first upper voltage value;

a fifth transistor having its gate connected to the input signal, its source connected to the voltage supply at the first upper voltage value and its drain connected to the source of the third transistor;[[,]]

a sixth transistor connected between the fourth transistor and the voltage supply at the first upper voltage value, the inverted version of the input signal being applied to the gate of the sixth transistor;

a seventh transistor connected in parallel with the third transistor between the fifth transistor and the first transistor, the inverted version of the input signal being applied to the gate of the seventh transistor; and

a latch circuit receiving the output signal and the inverted version of the output signal, wherein the input signal swings between a second upper voltage value and the lower voltage value, and the output signal swings between the first upper voltage value and the lower voltage value.

15. (Original) The level shifting device of claim 14, wherein the first transistor is a NMOS transistor, the second transistor is a NMOS transistor, the third transistor is a PMOS transistor, the fourth transistor is a PMOS transistor, and the fifth transistor is a PMOS transistor.

16. (Canceled)

17. (Currently Amended) The level shifting device of claim [[16]] 14, wherein the sixth transistor is a PMOS transistor, the first transistor is a NMOS transistor, the second transistor is a NMOS transistor, the third transistor is a PMOS transistor, the fourth transistor is a PMOS transistor, and the fifth transistor is a PMOS transistor.

18. (Currently Amended) The level shifting device of claim [[16]] 14, wherein the lower voltage value is ground level.

19. (Canceled).

20. (Currently Amended) The level shifting device of claim [[19]] 14, wherein the seventh transistor is a NMOS transistor, the first transistor is a NMOS transistor, the second transistor is a NMOS transistor, the third transistor is a PMOS transistor, the fourth transistor is a PMOS transistor, the fifth transistor is a PMOS transistor, and the sixth transistor is a PMOS transistor.

21. (Currently Amended) The level shifting device of claim [[19]] 14, further comprising an eighth transistor connected in parallel with the fourth transistor between the sixth transistor and the second transistor, the input signal being applied to the gate of the eighth transistor.

22. (Original) The level shifting device of claim 21, wherein the eighth transistor is a NMOS transistor, the first transistor is a NMOS transistor, the second transistor is a NMOS transistor, the third transistor is a PMOS transistor, the fourth transistor is a PMOS transistor, the fifth transistor is a PMOS transistor, the sixth transistor is a PMOS transistor, and the seventh transistor is a NMOS transistor.

23. (Canceled)

24. (Currently Amended) The level shifting device of claim [[23]] 29, wherein the sixth transistor is a NMOS transistor, the first transistor is a NMOS transistor, the second transistor is a NMOS transistor, the third transistor is a PMOS transistor, the fourth transistor is a PMOS transistor, and the fifth transistor is a PMOS transistor.

25. (Currently Amended) The level shifting device of claim [[23]] 29, further comprising a seventh transistor connected in parallel with the fourth transistor between the second transistor and the voltage supply at the first upper voltage value, the input signal being applied to the gate of the seventh transistor.

26. (Original) The level shifting device of claim 25, wherein the seventh transistor is a NMOS transistor, the first transistor is a NMOS transistor, the second transistor is a NMOS transistor, the third transistor is a PMOS transistor, the fourth transistor is a PMOS transistor, the fifth transistor is a PMOS, and the sixth transistor is a NMOS transistor.

27. (Original) The level shifting device of claim 14, wherein the latch circuit comprises a CMOS transistor configuration.

28. (New) A level shifting device, comprising:

a first transistor having its gate connected to an input signal, its source connected to a voltage node at a lower voltage value, and its drain connected to an output signal;

a second transistor having its gate connected to an inverted version of the input signal, its source connected to the voltage node at the lower voltage value, and its drain connected to an inverted version of the output signal;

a third transistor having its gate connected to the drain of the second transistor, and its drain connected to the drain of the first transistor;

a fourth transistor having its gate connected to the drain of the first transistor, its drain connected to the drain of the second transistor, and its source connected to a voltage supply at a

first upper voltage value;

a fifth transistor having its gate connected to the input signal, its source connected to the voltage supply at the first upper voltage value, and its drain connected to the source of the third transistor;

a sixth transistor connected in parallel with the third transistor between the fifth transistor and the first transistor, the inverted version of the input signal being applied to the gate of the sixth transistor;

wherein the input signal swings between a second upper voltage value and the lower voltage value and the output signal swings between the first upper voltage value and the lower voltage value.

29. (New) A level shifting device, comprising:

a first transistor having its gate connected to an input signal, its source connected to a voltage node at a lower voltage value, and its drain connected to an output signal;

a second transistor having its gate connected to an inverted version of the input signal, its source connected to the voltage node at the lower voltage value, and its drain connected to an inverted version of the output signal;

a third transistor having its gate connected to the drain of the second transistor, and its drain connected to the drain of the first transistor;

a fourth transistor having its gate connected to the drain of the first transistor, its drain connected to the drain of the second transistor, and its source connected to a voltage supply at a first upper voltage value;

a fifth transistor having its gate connected to the input signal, its source connected to the voltage supply at the first upper voltage value and its drain connected to the source of the third transistor;

a sixth transistor connected in parallel with the third transistor between the fifth transistor and the first transistor, the inverted version of the input signal being applied to the gate of the sixth transistor._and

a latch circuit receiving the output signal and the inverted version of the output signal, wherein the input signal swings between a second upper voltage value and the lower voltage value, and the output signal swings between the first upper voltage value and the lower voltage value.

30. (New) The level shifting device of claim 29, wherein the latch circuit comprises a CMOS transistor configuration.